REMARKS/ARGUMENTS

These remarks are made in response to the Office Action of March 25, 2004 (Office Action). As this response is not timely filed within the three-month statutory period, a one month extension of time is herein requested.

In paragraphs 2 and 3 of the Office Action, Claims 1-3, and 15 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Number 6,061,653 to Fisher, *et al.* (Fisher). In paragraph 4, Claim 4 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fisher. In paragraph 5, Claims 5-10, 12-14, and 17-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fisher in view of U.S. Patent Number 6,539,087 to Walsh, *et al.* (Walsh). In paragraph 6, Claims 11 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fisher in view of U.S. Patent Number 6,535,513 to Kao, *et al.* (Kao).

The Applicants have amended independent claims 1, 17, 18 and 20 in order to clarify aspects of the present invention. Support for this amendment can be found at page 10, lines 14-19, and at page 19, lines 12-21 of the Applicants' specification. Dependent claim 5 has been amended to conform with the amendments made to the independent claims. No new matter has been added in consequence of this amendment.

Prior to addressing the rejections on the art, a brief review of the Applicants' invention is appropriate. The Applicants have invented a speech processing board which has been optimized for use in high volume speech processing applications. The speech processing board can be deployed both in a conventional computer telephony (CT) architecture and in a voice over IP (VoIP) gateway/endpoint architecture. The speech processing board of the present invention also can accommodate multiple instances of text-to-speech (TTS) application tasks and small vocabulary speech recognition tasks.

Unlike conventional speech processing boards, the speech processing board of the present invention can include multiple processor modules each of which can execute multiple instances of full function, large vocabulary speech recognition tasks similar to those of a conventional speech recognition engine with shared memory. Moreover, the speech processing board of the present invention further includes a language model cache mapped to a common address space

such that the language model cache can be uniformly accessed by each of the multiple processor modules. Similarly, a method aspect of the present invention includes loading selected language models in a storage separate from the multiple processor modules such that the selected language models are uniformly accessed by each processor module at a common address.

Turning to the rejections on the art, claims 1-3, and 15 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Fisher. Fisher discloses a method of operating a speech recognition system. The method loads a speech model from a storage facility into a memory accessible by a processor. This loading step includes two steps. A first of these steps loads process-independent state data representative of the plurality of states of the speech model. A second of these steps loads process-specific state data representative of the plurality of states of the speech model. The speech recognition system then performs a first speech recognition process with the processor by accessing the process-independent state data and a first portion of the process-specific state data. The speech recognition system also performs a second speech recognition process with the processor, where the second process also accesses the process-independent state data but further accesses a second portion of the process-specific state data different that the first portion of the process-specific state data. The speech model data may be the states, transitions, and scores of a Hidden Markov Model or pointers to the model may be loaded. In response to a third recognition process, loading a third portion of process-specific data invalidates the first portion.

With respect to independent Claim 1, as amended, Fisher fails to disclose every feature of the Applicants' invention. For example, Fisher fails to teach the use of multiple memory processors that can each uniformly access a language model cache mapped to a common address space. Although Fisher discusses a speech recognition system that uses multiple digital signal processors (DSPs), Fisher nowhere describes or suggests that each of the DSPs accesses a single language model at a common address. To the contrary, Fisher explicitly teaches that processing efficiency is achieved by "separating portions of [speech processing models] into process-independent storage area 42*a* and process-specific storage area 42*b*." (Col. 6, lines 44-57.) Fisher may use a single physical device, but it uses distinct memory spaces for different portions of the model as well the speech data recognized using the model. (Col. 4, lines 15-32.) This

partitioning of language models into separate portions, each separately stored in a different memory space, is the converse of mapping a language model to a common address space as taught by Applicants' invention.

It is not surprising that Fisher fails to teach or inherently disclose a language model cache mapped to a common address space, since Fisher attempts to achieve processing efficiencies by separating speech data into different data types. This division is intended to reduce the amount of overall memory space needed by allowing stored data to be shared by different speech processes. This objective and approach, however, are far removed from the mapping of a language model to a common address space as recited in amended independent Claim 1. It follows therefore that Fisher fails to teach each feature recited in independent Claim 1, as amended. Therefore, Applicants respectfully request withdrawal of the 35 U.S.C. § 102(e) rejection with respect to amended independent Claim 1. Whereas dependent Claims 2, 3, and 15 each depend from Claim 1 and recite additional features, Applicant's respectfully request that the rejection regarding these claims similarly be withdrawn.

The Examiner has rejected claims 5-10, 12-14, and 17-21 under 35 U.S.C. § 103(a) as being unpatentable over Fisher in view of Walsh, and the Examiner has rejected claims 11 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Fisher in view of Kao. Regardless of whether the references are properly combinable, the combination of Fisher with Walsh as well as the combination of Fisher with Kao fails to teach every feature recited in the claims. For example, none of the references disclose expressly or implicitly a language model cache that communicatively links to a bridge and that is uniformly accessible by each of multiple processor modules at a common address, as recited in amended Claim 17. Nor do any of the references teach or suggest a selected language model that is uniformly accessible in a common address space by each of the multiple processor modules as recited in independent Claims 18 and 20, as amended. Neither Walsh nor Kao is cited as teaching or suggesting such a feature, and, as discussed above, Fisher in so far as it discloses a totally different approach can not be read as even implying such a feature. Therefore, since the references singly and jointly fail to teach every feature of the claimed invention, the Applicants respectfully request that the 35 U.S.C. § 103(a) rejection with respect to independent Claims 18 and 20 be withdrawn. Whereas the

remaining dependent claims each recite additional features, withdrawal of the 35 U.S.C. § 103(a) rejection of these claims is also respectfully requested.

Applicants believe that this application is now in full condition for allowance, which action is respectfully requested. Applicants request that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

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